FLIP-FLOPs

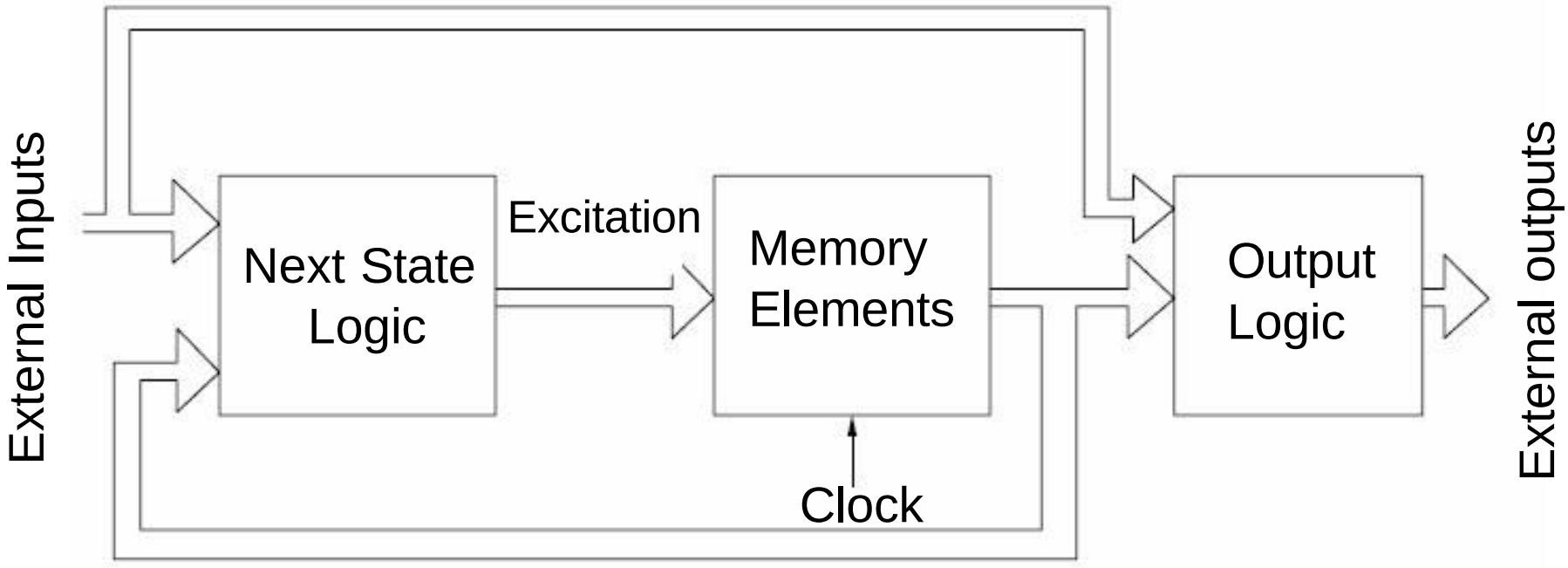


Fig. 7.1 *Block Diagram of a Sequential Circuit*

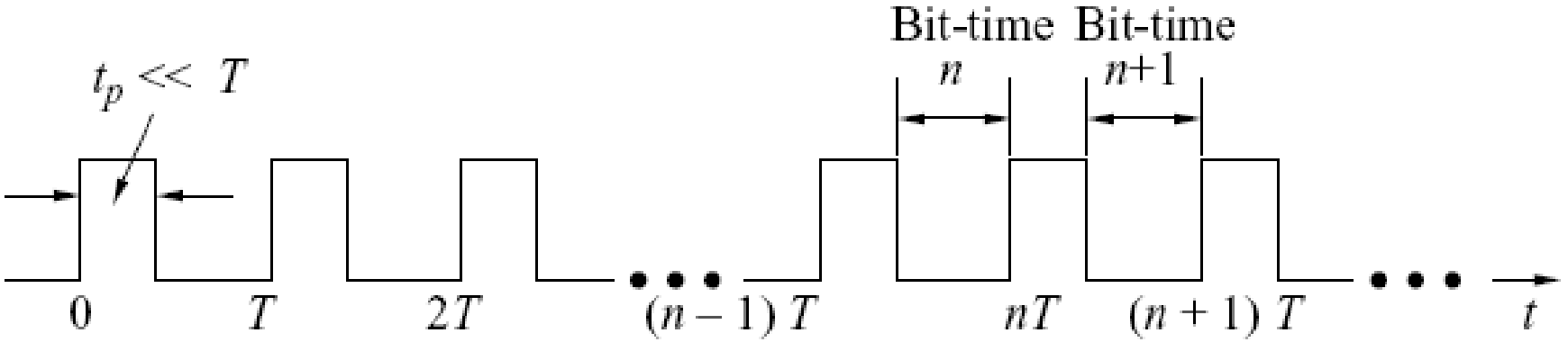


Fig. 7.2 ***A Train of Pulses***

A 1-BIT MEMORY CELL

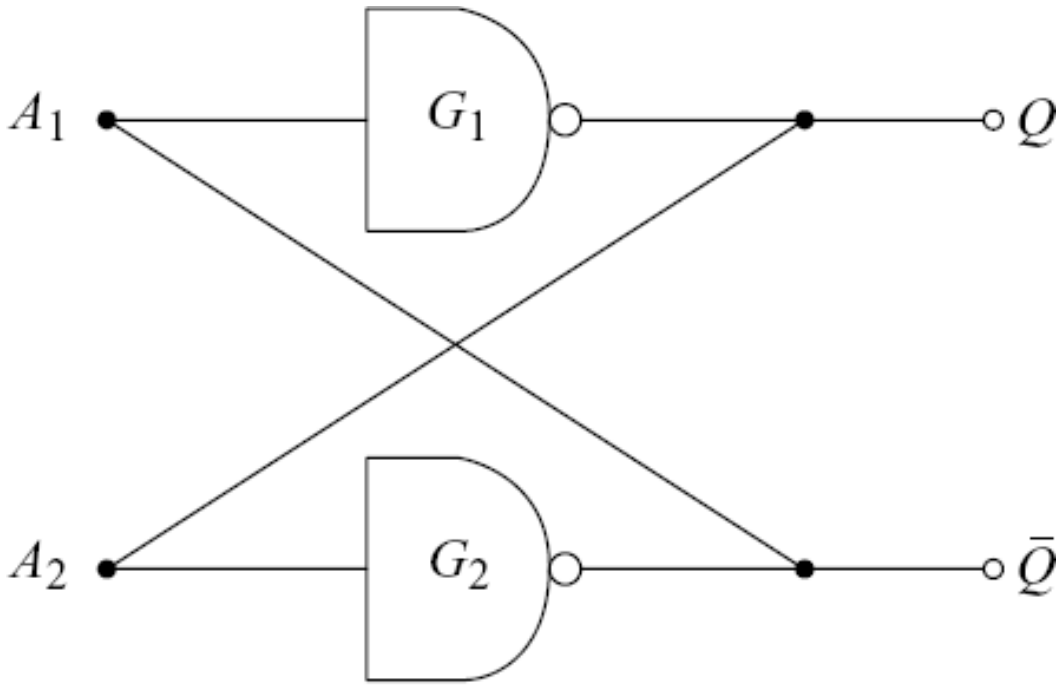


Fig. 7.3 ***Cross-coupled Inverters as a Memory Element***

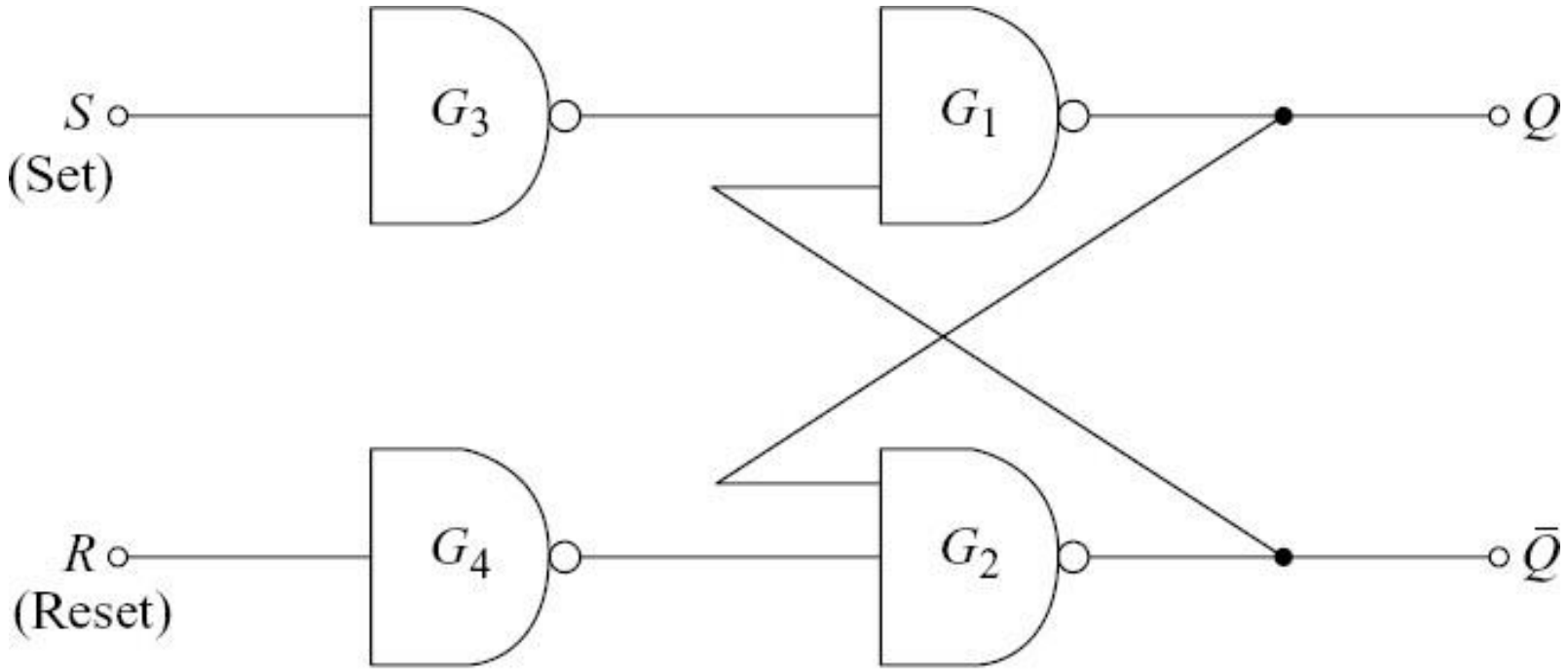


Fig. 7.4 ***The Memory Cell with Provision for Entering Data***

CLOCKED *S–R* FLIP-FLOP

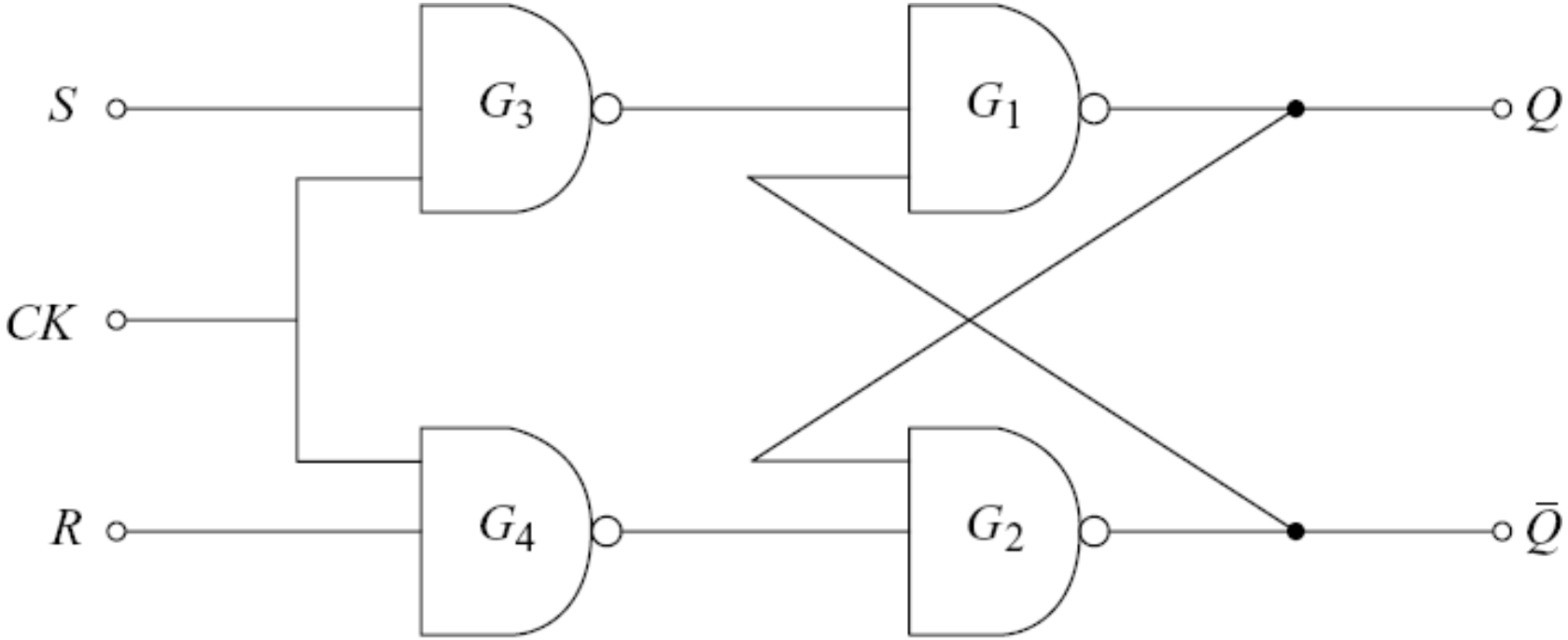


Fig. 7.5 ***A Clocked S–R*** FLIP-FLOP

Table 7.1 ***Truth Table of*** *S–R* FLIP-FLOP

Inputs		Output
S_n	R_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	?

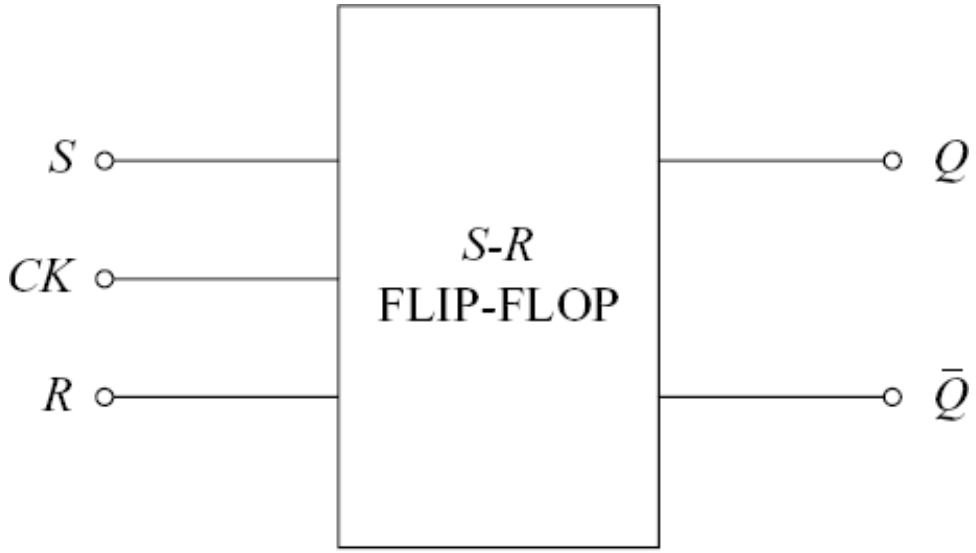


Fig. 7.6 ***Logic Symbol of Clocked*** *S–R* FLIP-FLOP

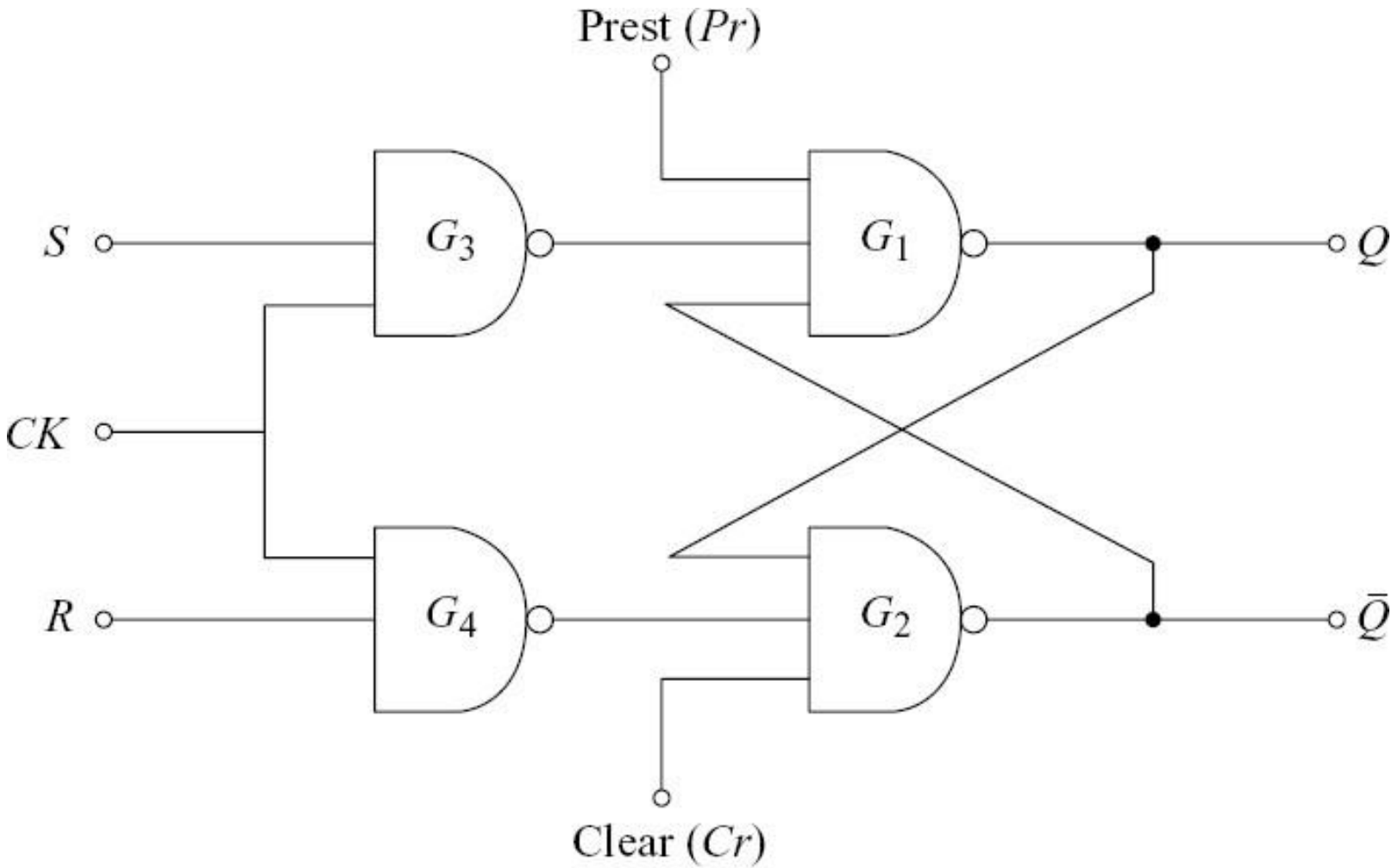


Fig. 7.7 ***(a) An S–R*** `FLIP-FLOP` ***with Preset and Clear, (b) Its Logic Symbol***

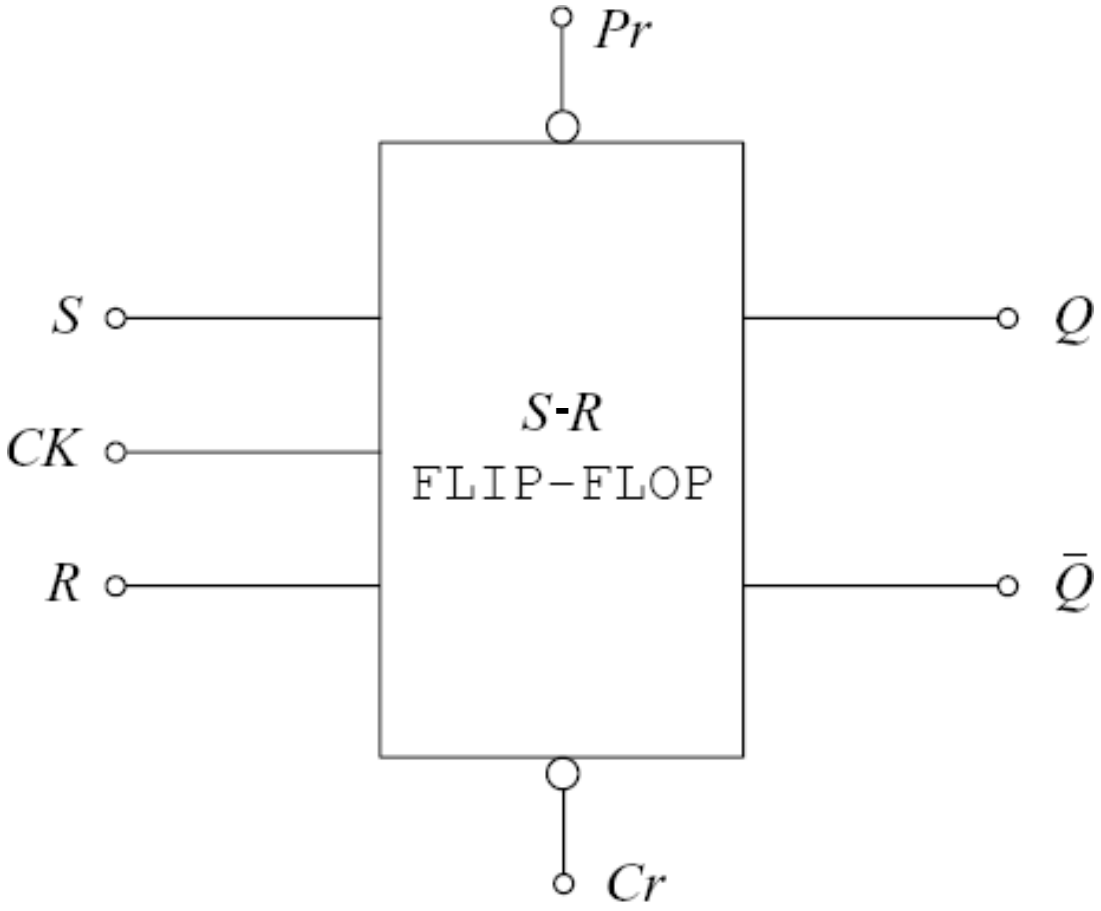


Fig. 7.7 ***(Continued)***

Table 7.2 ***Summary of Operation of S–R FLIP-FLOP***

Inputs			Output	Operation performed
CK	***Cr***	***Pr***	***Q***	
1	1	1	Q_{n+1}(Table 7.1)	Normal FLIP-FLOP
0	0	1	0	Clear
0	1	0	1	Preset

J-K FLIP-FLOP

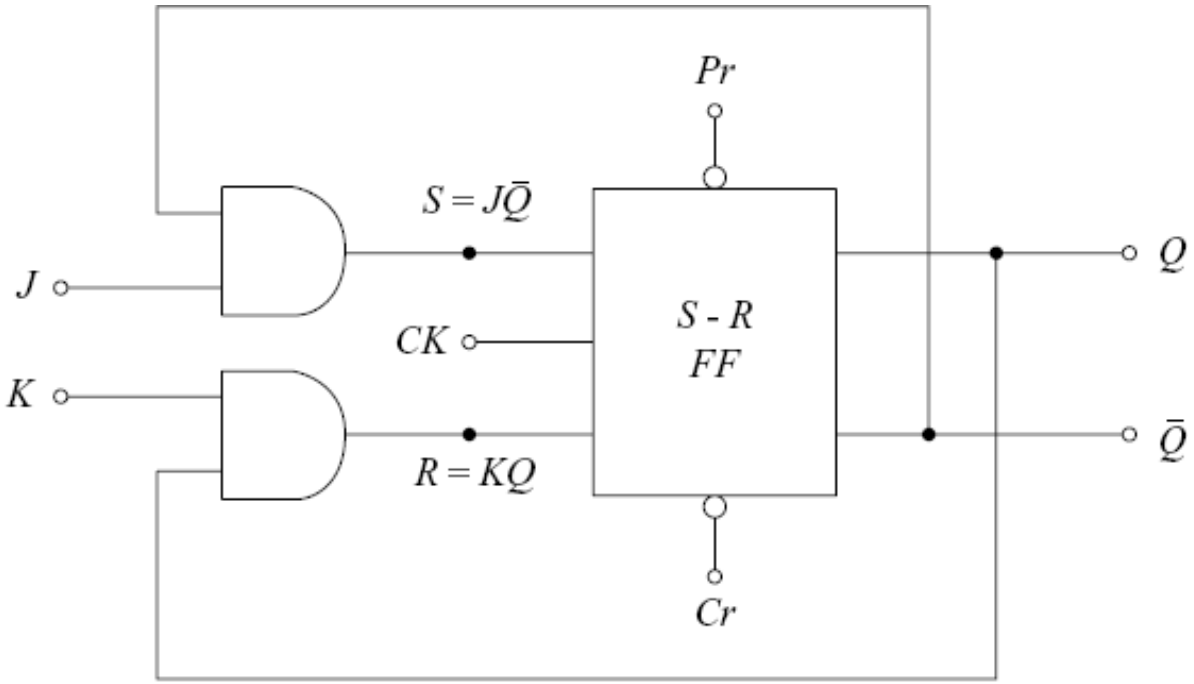


Fig. 7.8 ***An S–R FLIP-FLOP Converted into J–K FLIP-FLOP***

Table 7.3a ***Truth Table for Fig. 7.8***

Data inputs		Outputs		Inputs to S–R FF		Output
J_n	K_n	Q_n	$\overline{Q}_n$	S_n	R_n	Q_{n+1}
0	0	0	1	0	0	$\left.\begin{matrix}0\\1\end{matrix}\right] = Q_n$
0	0	1	0	0	0	
1	0	0	1	1	0	$\left.\begin{matrix}1\\1\end{matrix}\right] = 1$
1	0	1	0	0	0	
0	1	0	1	0	0	$\left.\begin{matrix}0\\0\end{matrix}\right] = 0$
0	1	1	0	0	1	
1	1	0	1	1	0	$\left.\begin{matrix}1\\0\end{matrix}\right] = \overline{Q}_n$
1	1	1	0	0	1	

Table 7.3b ***Truth Table of*** *J–K* FLIP-FLOP

Inputs		Output
J_n	K_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

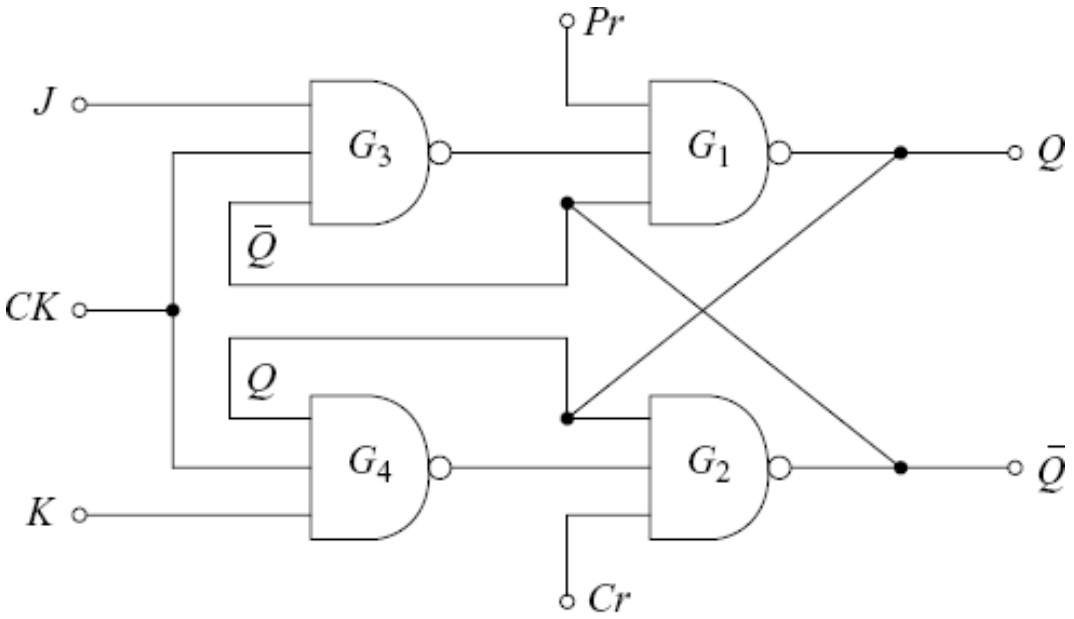


Fig. 7.9 ***A J–K*** `FLIP-FLOP` ***Using*** `NAND` ***Gates***

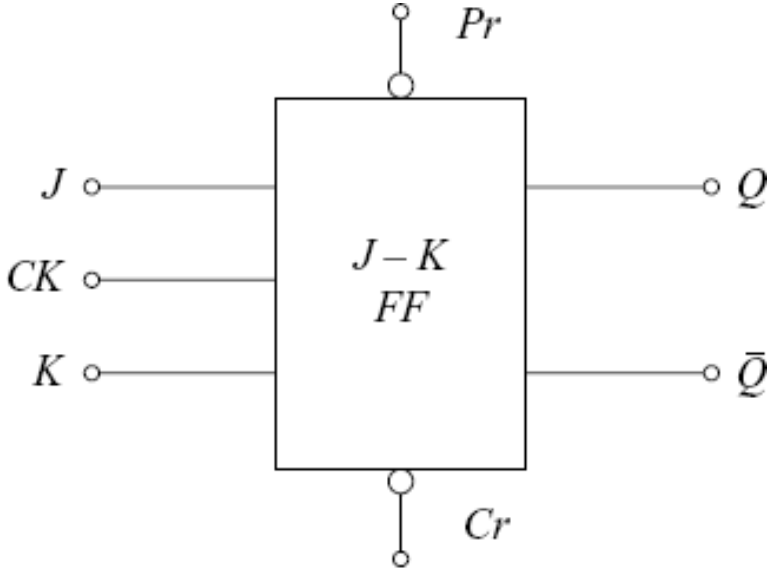


Fig. 7.10 ***Logic Symbols of J–K*** `FLIP-FLOP`

The Master–Slave *J–K* FLIP-FLOP

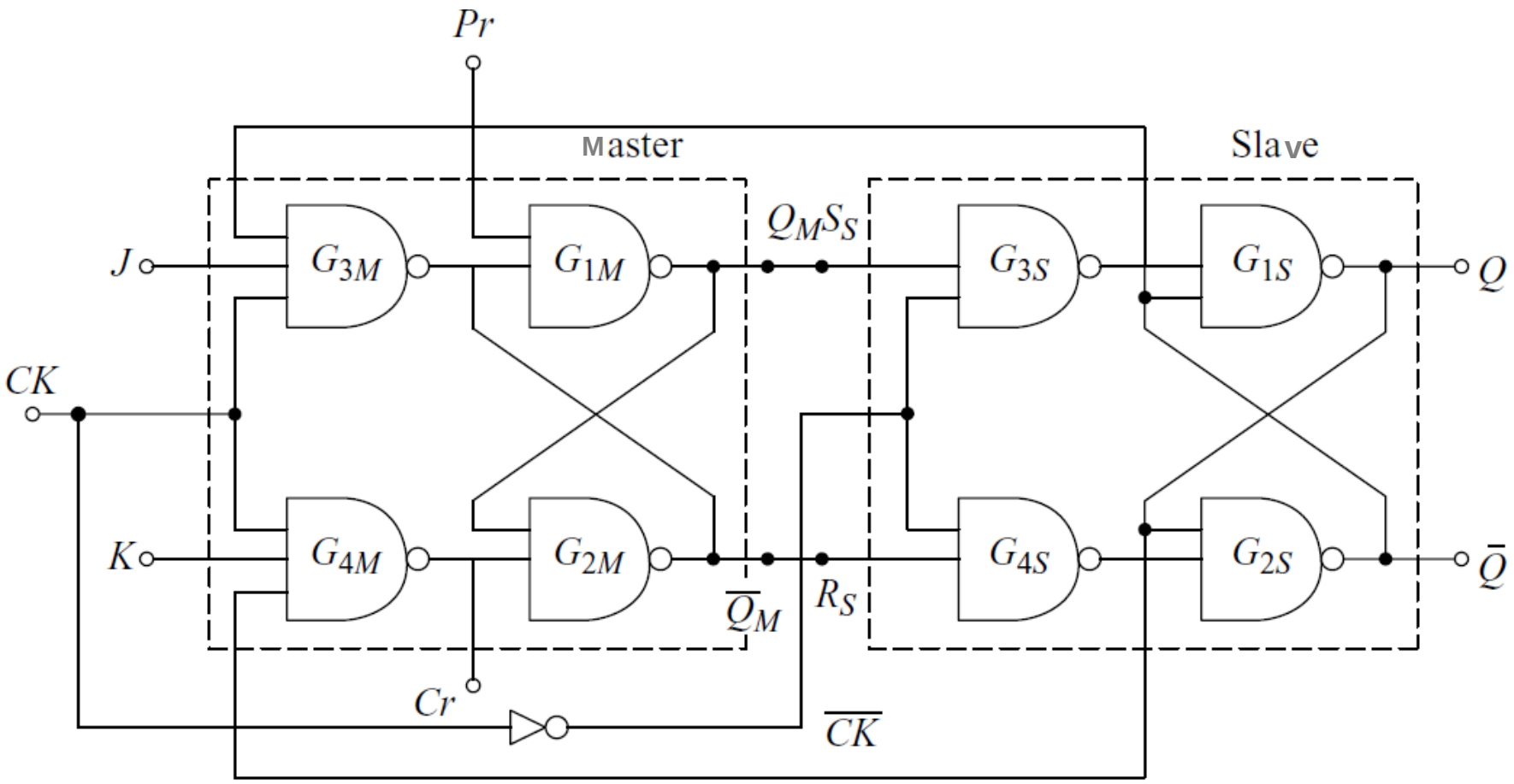


Fig. 7.12 ***A Master–Slave J–K*** FLIP-FLOP

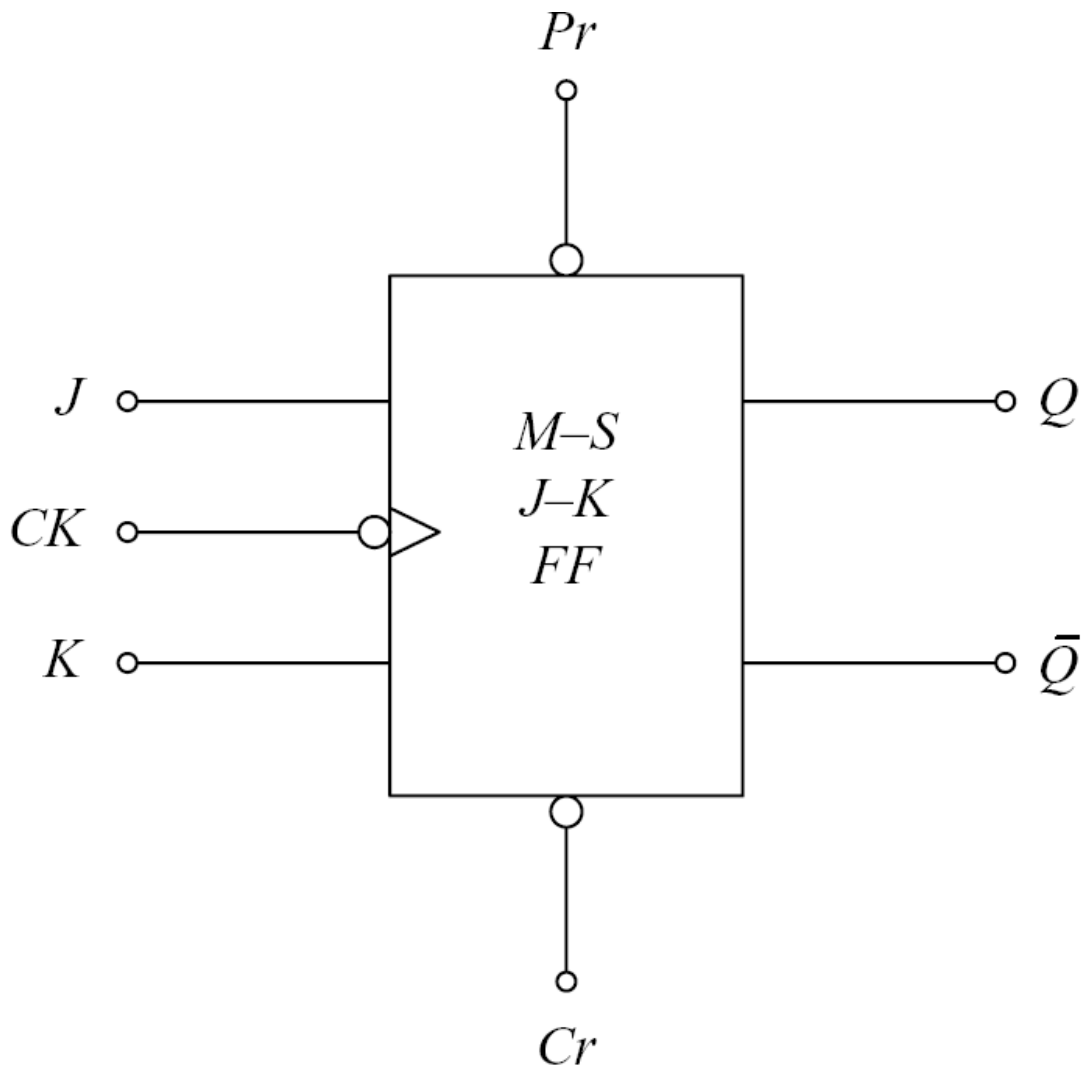


Fig. 7.13 ***A Master–Slave J–K*** `FLIP-FLOP` ***Logic Symbol***

D-**TYPE** FLIP-FLOP

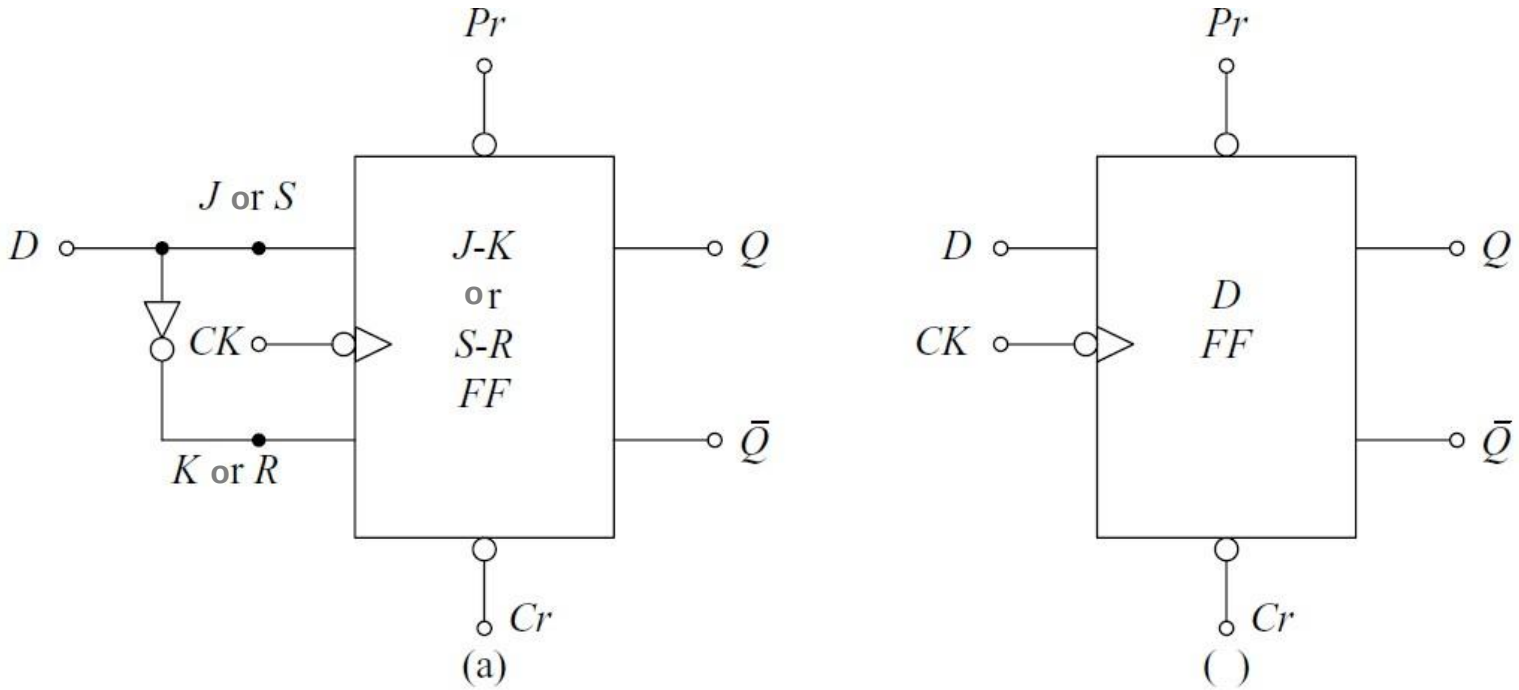


Fig. 7.14 ***(a) A J–K or S–R*** FLIP-FLOP ***Converted into a D-type*** FLIP-FLOP ***(b) its Logic Symbol***

Table 7.4 ***Truth Table of a D-type*** FLIP-FLOP

Input D_n	**Output** Q_{n+1}
0	0
1	1

T-**TYPE** FLIP-FLOP

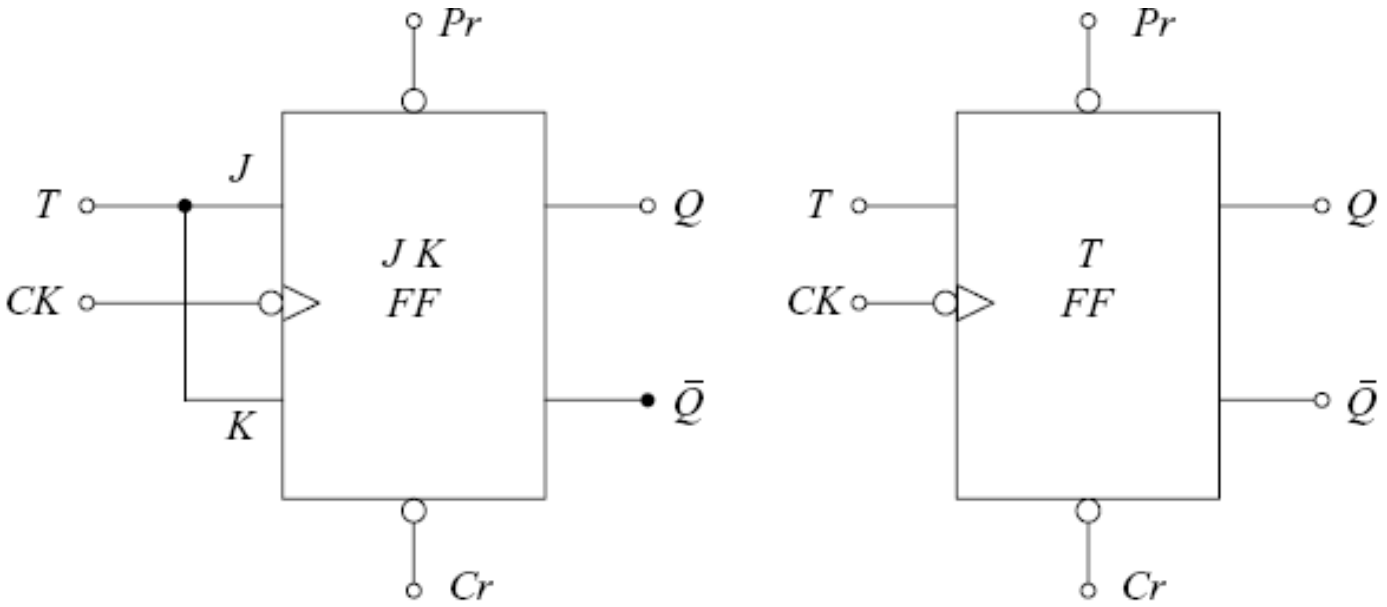


Fig. 7.15 ***(a) A J–K*** `FLIP-FLOP` ***Converted into a T-type*** `FLIP-FLOP` ***(b) its Logic Symbol***

Table 7.5 ***Truth Table of T-type*** `FLIP-FLOP`

Input T_n	**Output** Q_{n+1}
0	Q_n
1	$\overline{Q}_n$

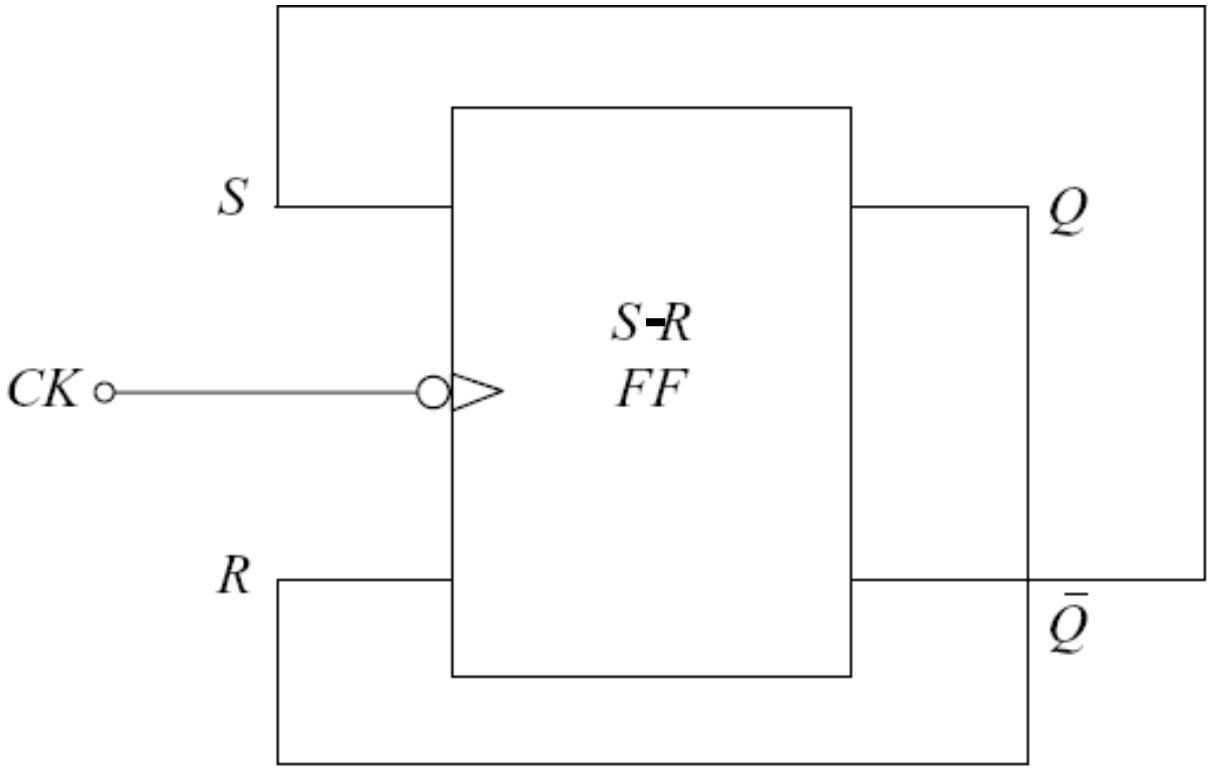


Fig. 7.16 ***An S–R*** `FLIP-FLOP` ***as a Toggle Switch***

EXCITATION TABLE OF FLIP-FLOP

Table 7.6 ***Excitation Table of* FLIP-FLOPs**

Present State	Next State	*S–R FF*		*J–K FF*		*T-FF*	*D-FF*
		S_n	R_n	J_n	K_n	T_n	D_n
0	0	0	×	0	×	0	0
0	1	1	0	1	×	1	1
1	0	0	1	×	1	1	0
1	1	×	0	×	0	0	1

CLOCKED FLIP-FLOP **DESIGN**

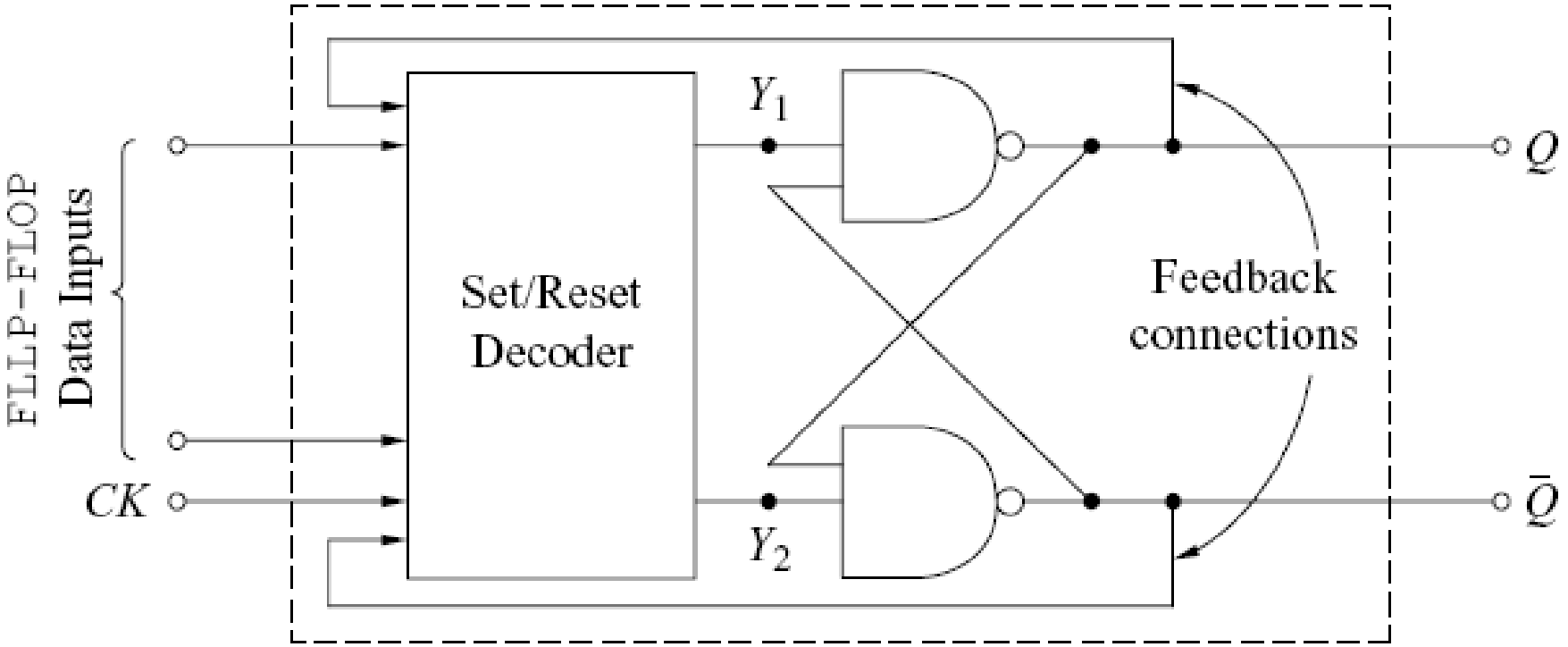


Fig. 7.17 ***The General Model of the*** FLIP-FLOP

Conversion from One Type of FLIP-FLOP to Another Type

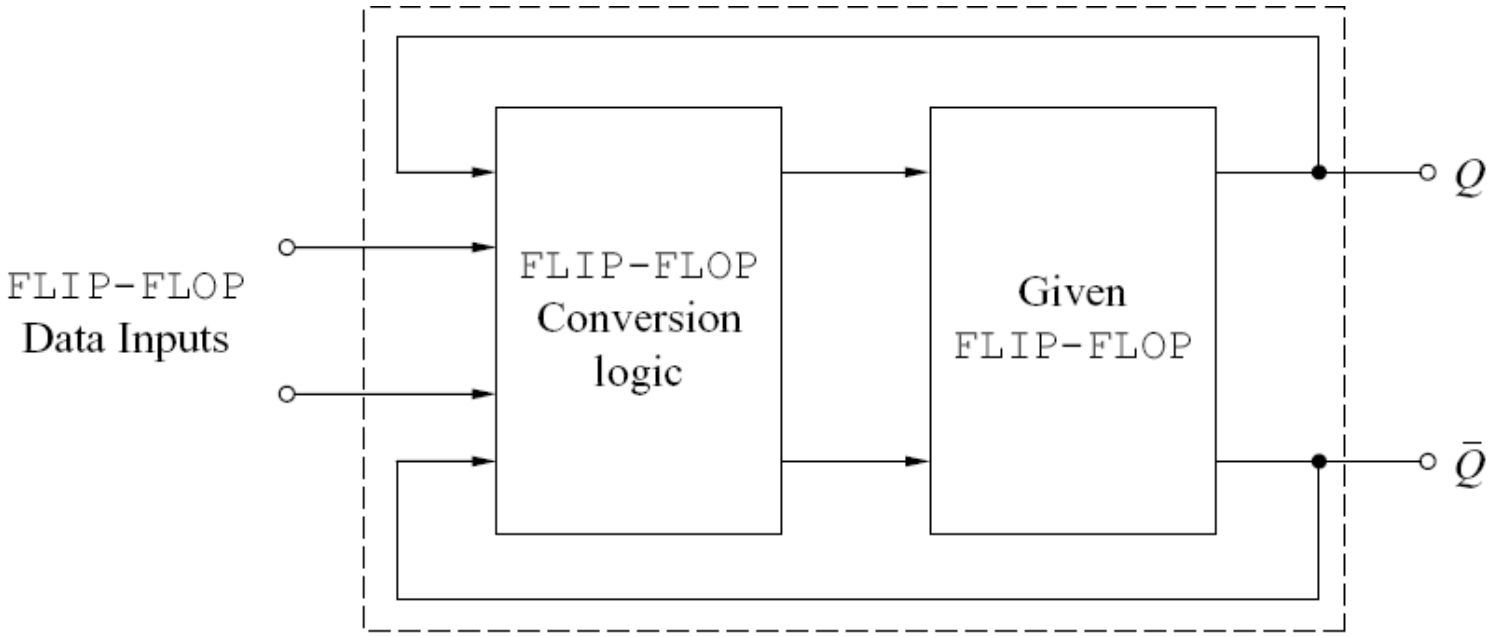


Fig. 7.19 ***The General Model Used to Convert One Type of*** FLIP-FLOP ***to Another Type***

EDGE-TRIGGERED FLIP-FLOPs

Set-up time (t_s)

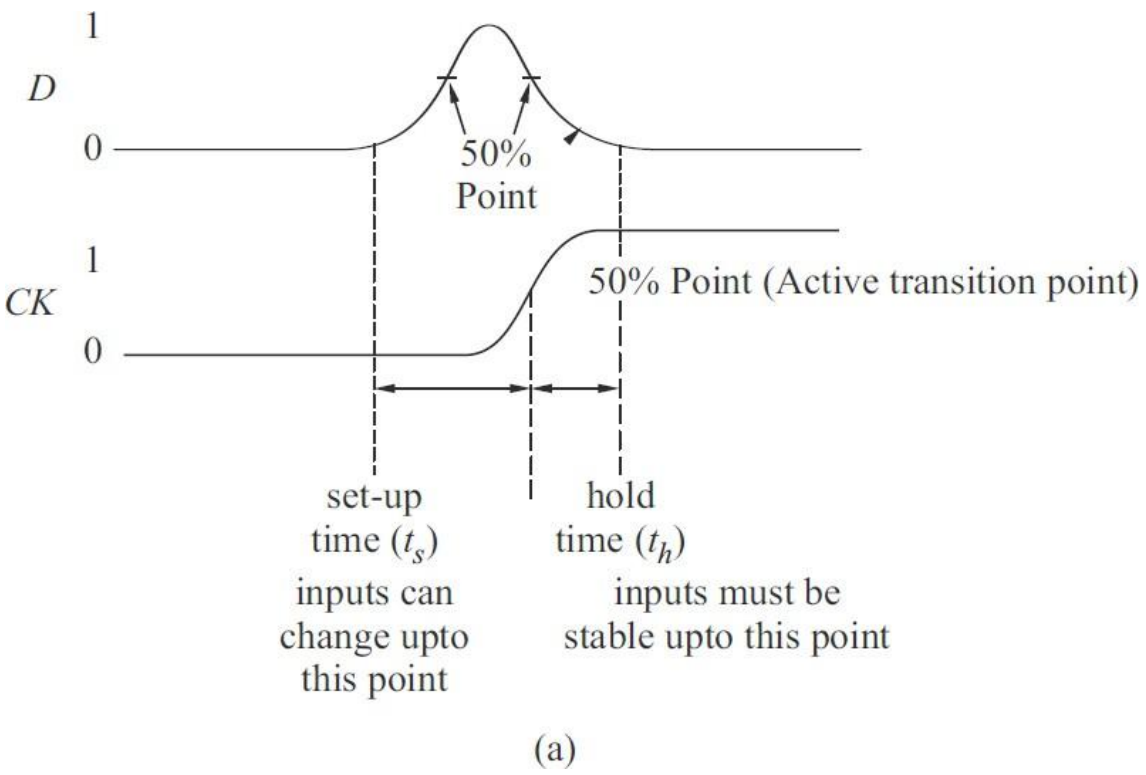
Hold time (t_h)

Propagation Delays

Clock Pulse Width

Preset and Clear Pulse Width

Maximum Clock Frequency



(a)

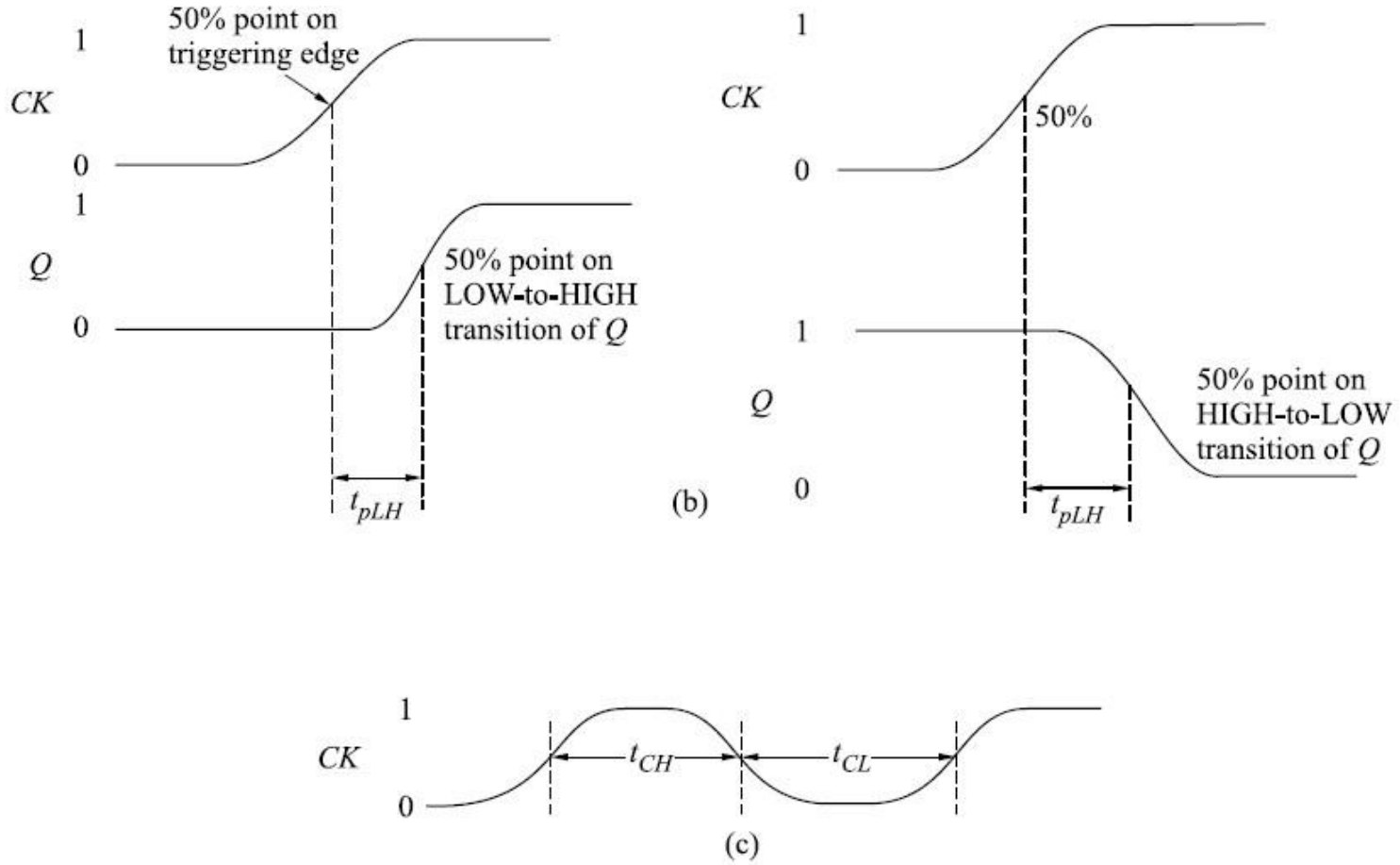


Fig. 7.21 FLIP-FLOP ***Timings (a) Set-up and Hold Timings (b)Propagation Delays (c) Clock*** LOW ***and*** HIGH ***Timings***

Timing Parameters of TTL **and** CMOS FLIP-FLOP**s**

	TTL			CMOS			
Parameter	**74LS74A**	**74LS112**	**74F74**	**74HC74A**	**74HC112**	**74AHC74**	**UNIT**
t_s (set up time)	20	20	2	14	25	5	ns
t_h (hold time)	5	0	1	3	0	0.5	ns
t_{pHL} (*CK* to *Q*)	40	24	6.8	17	31	4.6	ns
t_{pLH} (*CK* to *Q*)	25	16	8	17	31	4.6	ns
t_{pHL} (*Cr* to *Q*)	40	24	9	18	41	4.8	ns
t_{pLH} (*Pr* to *Q*)	25	16	6.1	18	41	4.8	ns
t_{CH} (clock HIGH time)	25	20	4	10	25	5	ns
t_{CL} (clock LOW time)	25	15	5	10	25	5	ns
t_{WL} (*Pr* or *Cr* LOW time)	25	15	4	10	25	5	ns
f_{MAX} (Max. frequency)	25	30	100	35	20	170	MHz

APPLICATIONS OF FLIP-FLOP**s**

1. Bounce elimination switch,
2. Latch,
3. Registers,
4. Counters,
5. Memory, etc.

Bounce-Elimination Switch

Example 7.4

Show that the circuit of Fig. 7.23*a* acts as a bounce-elimination (chatterless) switch.

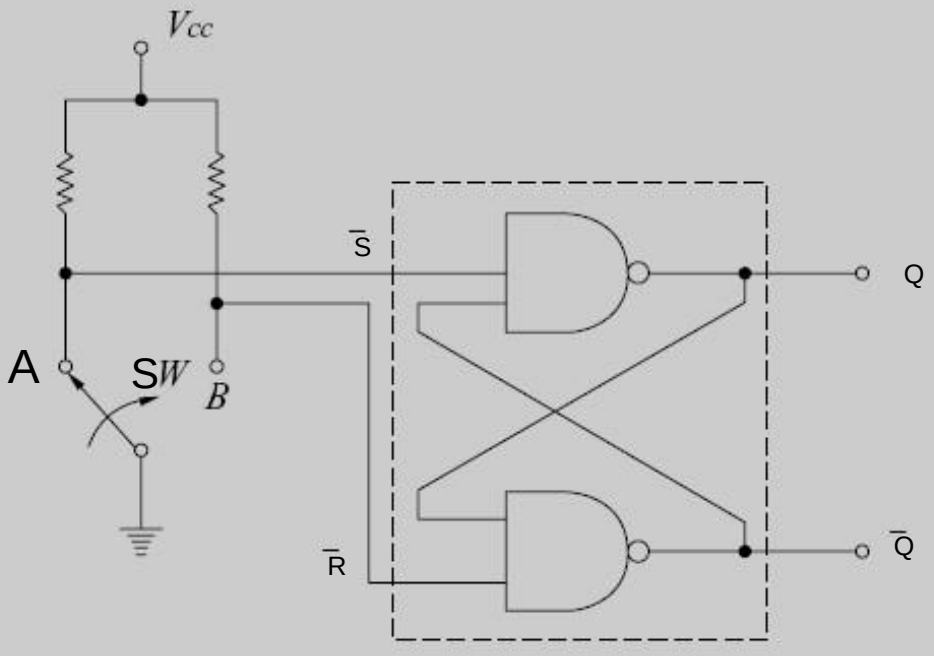
Solution

The waveforms at $\overline{S}$, $\overline{R}$, Q, and $\overline{Q}$ are illustrated in Fig. 7.23*b*. The switch (SW) is thrown from position A to B at $t = 0$. Therefore, at $t = 0^+$ the voltage at $\overline{S}$ will be V_{CC} (logic 1) and will continue to remain so as long as the switch is not thrown to position A again.

At $\overline{R}$ (B), the voltage at $t = 0^-$ is V_{cc} (logic 1) and goes to 0 V (logic 0) at t_1 (t_1 being the time delay of the switch). The switch arm makes contact at B at $t = t_1$, and then bounces off. Therefore, the level at $\overline{R}$ changes from 0 to 1 and vice-versa. This is illustrated in Fig. 7.23*b*.

Between $t = 0$ and $t = t_1$, both the inputs $\overline{S}$ and $\overline{R}$ are at logic 1 and therefore, Q does not change. The output Q changes at t_1 and becomes 0. Now, even when $\overline{R}$ is changing at t_2, t_3, etc. Q does not change. This shows that it is a chatterless switch.

The latch used in Fig. 7.23*a* can be replaced by the IC 74279 which is a quad $\overline{S} - \overline{R}$ latch.



(a) Latch

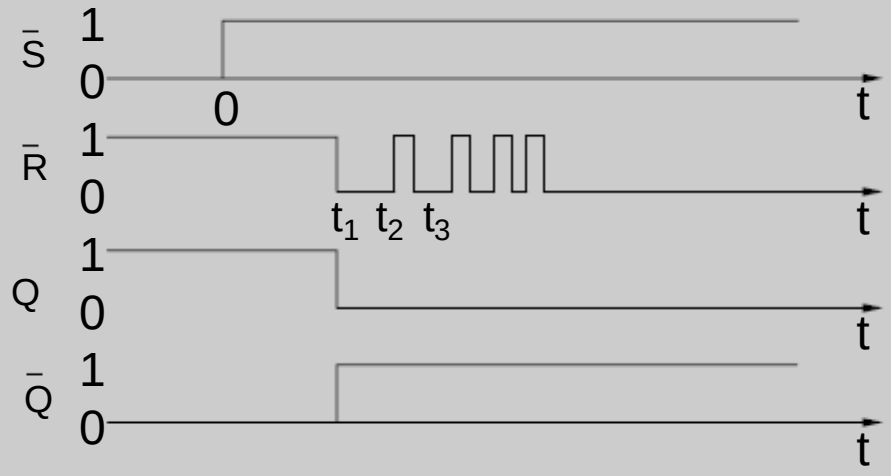


Fig. 7.23 *(a) A Bounce-Elimination Switch (b) Waveforms of $\bar{S}$, $\bar{R}$, Q, and $\bar{Q}$*

Registers

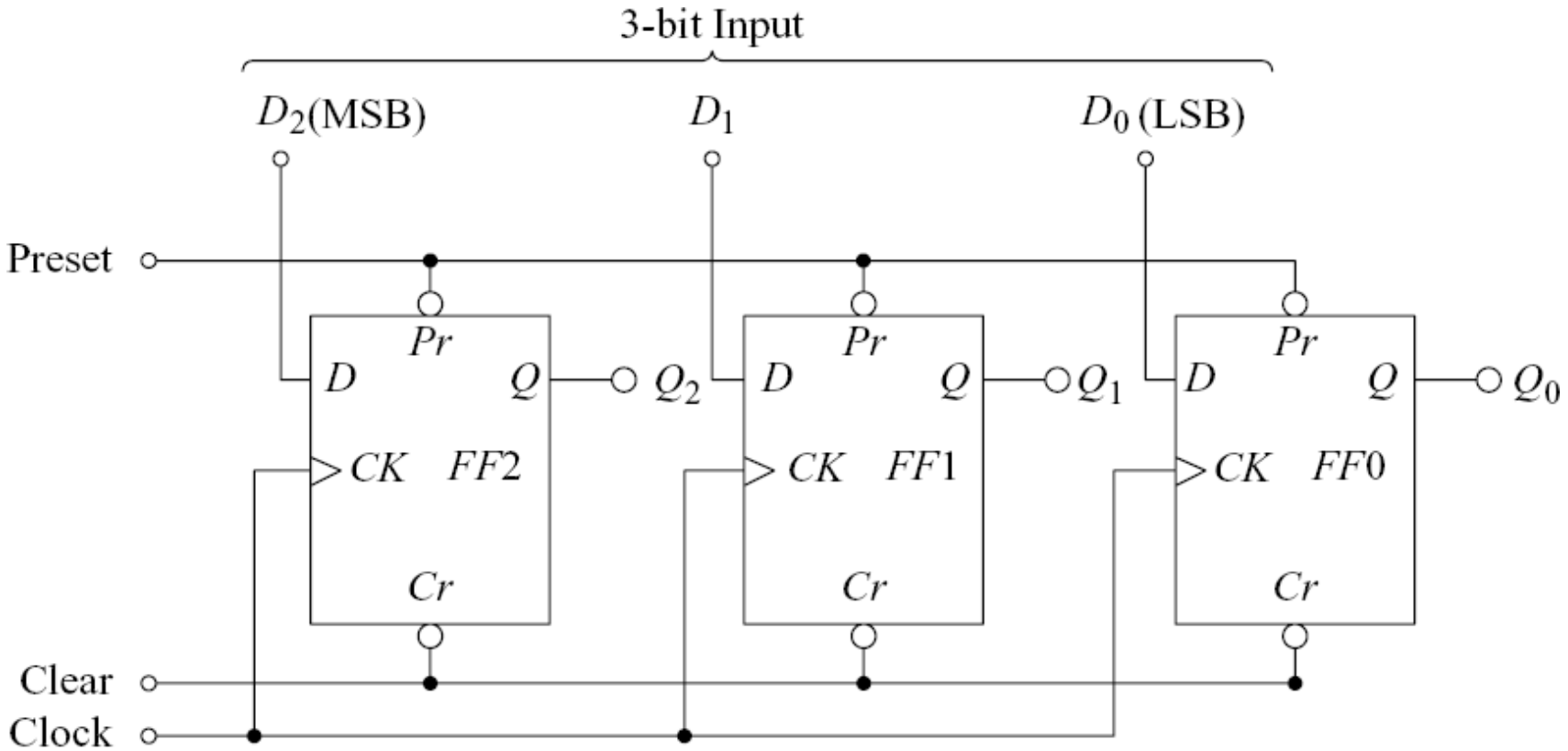


Fig. 7.24 ***A 3-bit Register Using*** `FLIP-FLOPs`

Counters

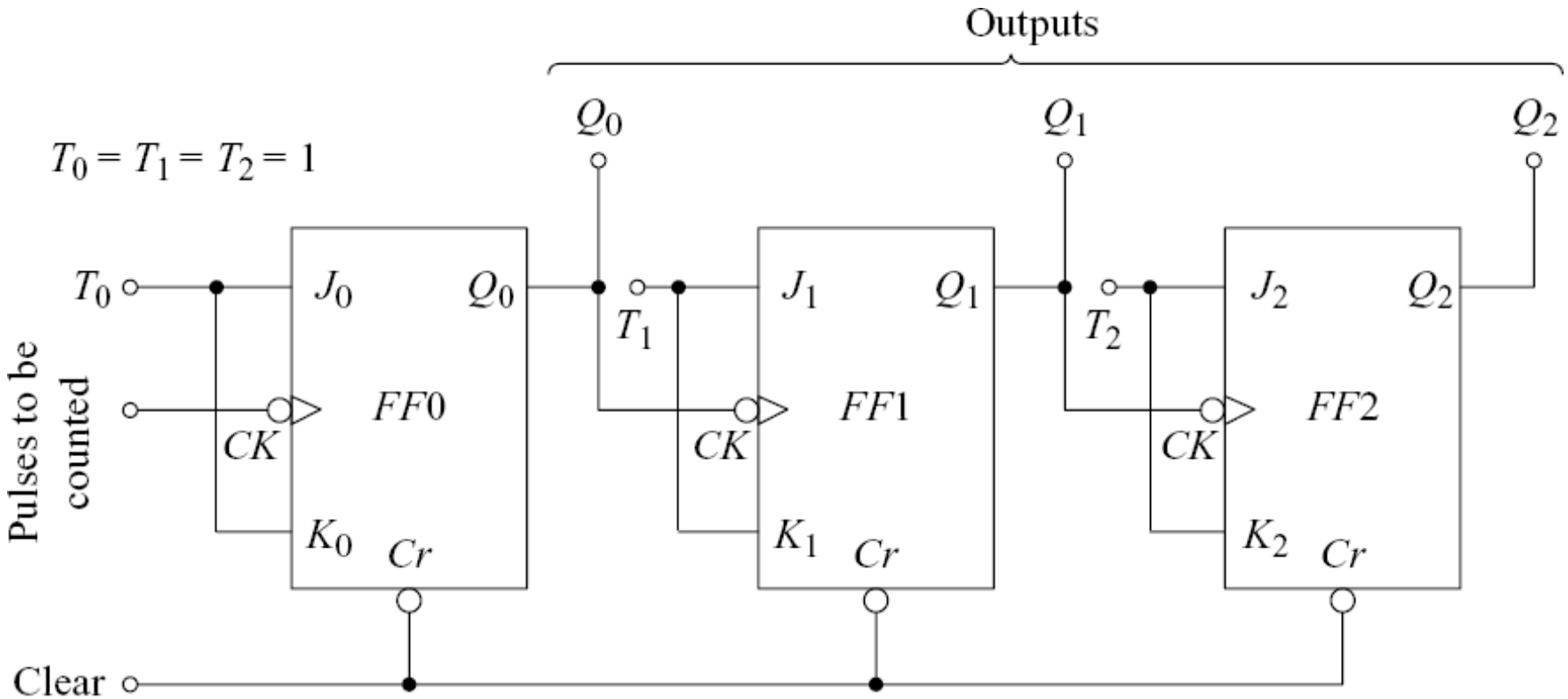


Fig. 7.25 ***A 3-bit Counter Using*** FLIP-FLOPs

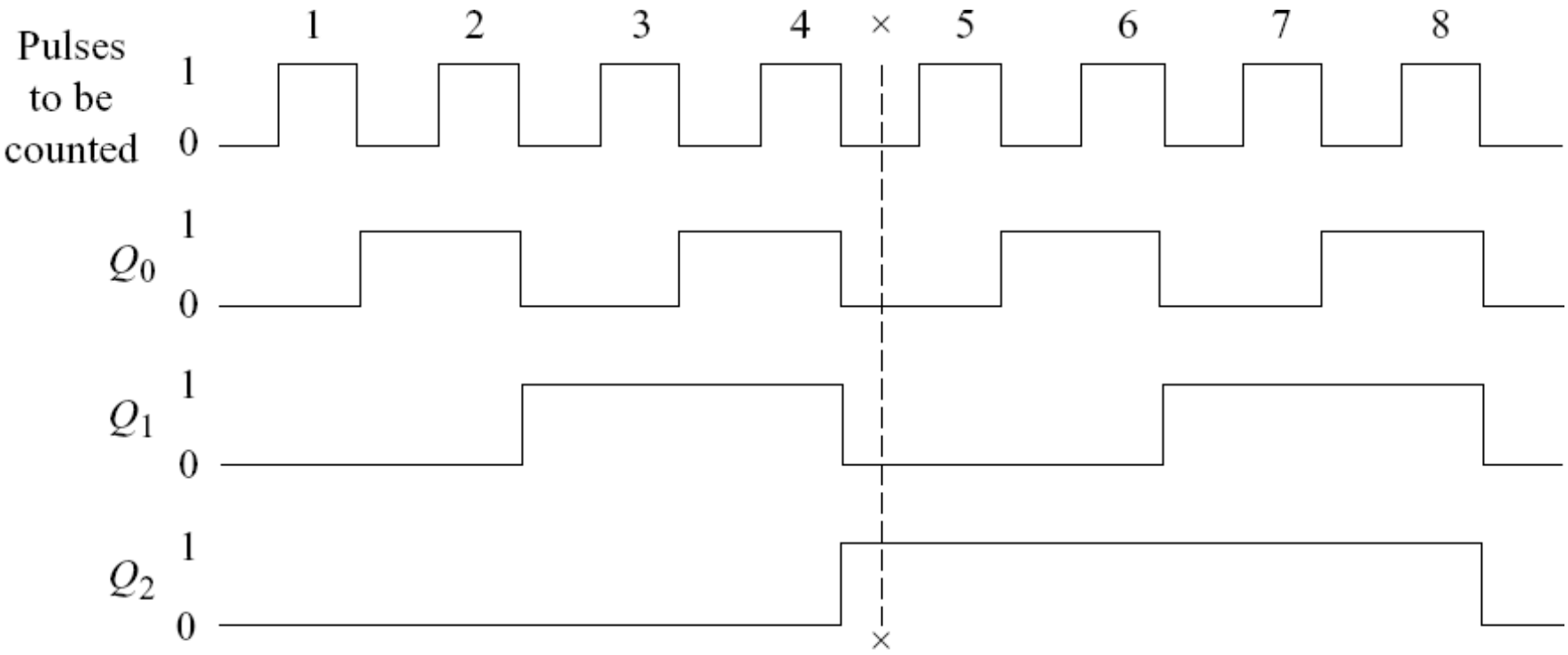


Fig. 7.26 ***Waveforms of Counter of Fig. 7.25***

Random-Access Memory

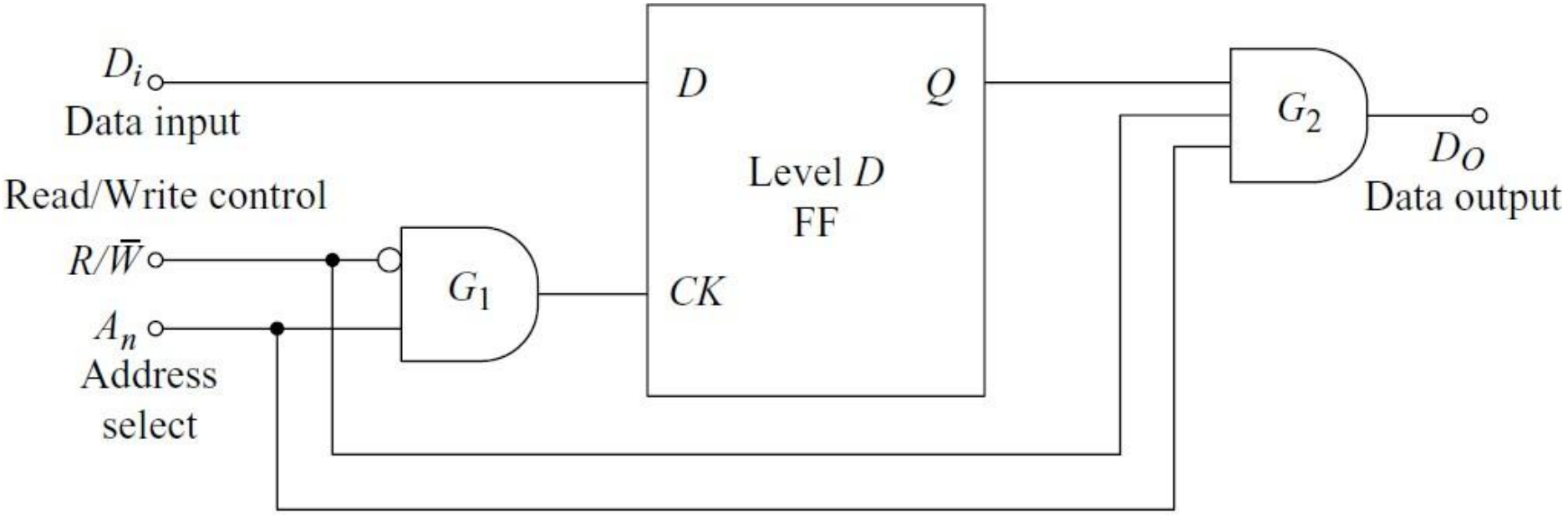


Fig. 7.27 ***A 1-bit Read/Write Memory Cell***

Table 7.10 ***Function Table of 1-bit Memory Cell***

Inputs			Mode
A_n	$R/\overline{W}$	D_i	
0	×	×	Hold, $D_0 = 0$
1	0	0	Write 0 into memory, $D_0 = 0$
1	0	1	Write 1 into memory, $D_0 = 0$
1	1	×	Read, D_0 = stored D_i bit.